REMARKS/ARGUMENTS

In view of the amendments and remarks presented herein, favorable consideration and allowance of this application are respectfully requested.

Claims 30 and 31 are canceled without prejudice or disclaimer.

An Information Disclosure Statement was filed by Applicant on April 6, 2009 that was not acknowledged by the Examiner in the last Official Office Action. Applicant respectfully requests that the Examiner consider and acknowledge consideration of the references recited in Applicant's IDS filed April 6, 2009.

Applicant also respectfully requests the Examiner to acknowledge and consider all the documents submitted in the IDS filed 9/20/2006. A concise explanation of relevance of these documents is evident from the partial translations and English Abstracts submitted in the 9/20/2009 IDS. In this regard, Applicant wishes to point out that the two NPL documents "A speedup Technique with Function Level Value Reuse and Parallel Precomputation" and "Information Processing society of Japan Journal: High Performance Computing System" are actually one and the same document for which a partial translation with respect to relevant Figures 1, 3 and 4 was submitted in Applicant's 9/20/2009 IDS. Also, in regards to the KR 10-2005-0108343A reference, the corresponding English US Patent Publication US2006/0050779 was submitted in the IDS filed 2/12/2009.

Applicant respectfully submits that the current specification meets the requirements of 37 CFR 1.52(a) and (b) and that a substitute specification is neither warranted nor required. If the Examiner knows of any specific incidences of egregious non-idiomatic English or other errors which are in need of correction/clarification or other changes/corrections which should be

implemented in Applicant's specification, please indicate such in the next official action so that Applicant can take appropriate measures to clarify or correct.

Applicant respectfully traverses the Examiner's objection to claims 16-17 as being in improper form. Claims 16-17 do not reference a multiple dependent claim because Applicant's claim 15, on which these claims depend, was amended via the September 20, 2009 Preliminary Amendment to depend solely on claim 1. Applicant also respectfully traverses the Examiner's objection to claims 30 and 31 because these claims are hereby canceled as indicated above.

Regarding the 35 U. S. C. § 112, First Paragraph Rejection:

Within the Office Action, claims 1-17 were rejected under 35 U.S.C. §112, 1st paragraph, as allegedly containing subject matter which was not described in the specification in such a way as to enable one of ordinary skill in the art to practice the invention. In particular, it is stated that "the i/o group which is made up of input/output pattern was not described in the specification in such a way as to enable one skilled in the art to which it pertains..." and that "The specification merely recites same limitation but did not describe it in the specification in such a way as to enable one of ordinary skill in the art to which it pertains." In addition, Office Action further alleges that the specification merely recites "matching pattern", "performing reuse", "input/output element" and "pattern derives" but does not describe these elements in such a way to enable one skilled in the art to make and/or use the invention. The Office Action also alleges that the limitations recited in claims 2 and 3 are merely recited the same in the specification but are not described in such a way to enable one skilled in the art to which it pertains.

Applicant respectfully traverses these rejections for at least the following reasons: In regard to the I/O group as recited in claim 1, Applicant respectfully directs the Examiner's

attention, with reference to Figure 10 of Applicant's specification, to at least the description of the I/O group found in Applicant's specification at page 104, paragraph 3 et seq., and to the discussion of the setting of the I/O group found in Applicant's specification at page 114, first paragraph, through the second paragraph of page 118. Likewise, the Examiner's attention is directed toward Applicant's specification at pages 73 through 77 with reference to Figure 3, which describes in greater detail at least one non-limiting example implementation of matching an input pattern and the performing of a "reuse" operation, in addition to describing other claim elements concerning an "input/output element" and how a "pattern derives" as set forth in Applicant's dependent claims 2 and 3. Applicant respectfully contends that at least these above mentioned example sections of Applicant's specification, among other sections, are sufficiently enabling to allow one skilled in the art to practice these aspects of the claims without undue experimentation and do not merely parrot the claim language.

Regarding the 35 U. S. C. § 112, 2nd ¶, Rejection:

Within the Office Action, claims 1-17 were rejected under 35 U.S.C. §112, 2nd paragraph, as allegedly being indefinite. By this amendment, applicant has amended independent claim 1, and dependent claims 2, 3 and 6-17, to more clearly set forth and distinctly claim all features and language identified by the Examiner as being vague or indefinite or lacking antecedent basis (i.e., Office Action at items 18-24), including claim features concerning Applicant's "input/output group", "input pattern" and an associated "output pattern", "input elements" and "output elements". Moreover, example implementations of these elements and terms in Applicant's claims are described, as mentioned above, in greater detail in Applicant's specification with reference to the corresponding Figures (see, e.g., Figure 10 of Applicant's

specification and pages 104 and 115-118 regarding I/O group; and pages 73-86 regarding registering an input pattern, matching an input pattern to a sequence of stored instructions stored and conducting a "resue" of output from previously executed instructions).

For example, Applicant's specification at page 103, line 20, through page 104, line 2, with reference to Figure 10, indicates that the "rows AND comparison section" (MR) is an example of the claimed "input/output group setting means" and explains that "[t]he rows AND comparison section MR is a computation section that performs an AND operation on row elements stored in the dependency relations storage section M, and sets an *input/output group made up of: an output pattern including at least one output address and output value; and an input pattern including at least one input address and input value.*"

Also, regarding the input pattern, see for example, Applicant's specification at page 108, line 5 et seq., which explains:

> "With this, *a pattern of input addresses/values*, from which an output with respect to output addresses/values having been registered in the RWO derive, *is represented by the row element, of the dependency relations storage section M,* which corresponds to the output address."

...also, Applicant's specification at page 115, lines 4 et seq. explains:

> "Since the dependency relations storage section M is generated as above, the following information is obtained when the execution of an instruction region is completed.
>
> (Rs1) In a row element of the dependency relations storage section M, an input address/value *from which a corresponding output address/value derives* is 1.
>
> (Rs2) If , in a row element Ma, a group of input addresses/values that are 1 forms one input group, and the input group is matched, a reusable output address/value is an output address/value corresponding to the row element Ma.
>
> (Rs3) If a logical AND of "an inversion of a row element Ma" and "a row element Mb" is all 0, a pattern of 1 in the Ma includes a pattern of 1 in the Mb. That is, a group of input addresses/values belonging to the Ma forms one input group, *and a reusable output address/value* in a case where the input group is matched *is an output address/value corresponding to the Ma and an output address/value corresponding to the Mb.*"

...and, Applicant's specification at page 118, lines 8 et seq. further explains:

> "When input/output groups are set as above, the rows AND comparison section MR assigns group IDs to the respective input/output groups, and stores, in a group ID storage section ID, information which indicates in which group ID each input address/value registered in the RWI is included. As a result, it is possible to specify an input pattern of each input/output group, by referring to the content of the group ID storage section ID."

Regarding the meaning of performing a "reuse" operation, Applicant's specification describes the conventional meaning of a value reuse operation:

> "Aside from the branch prediction, there has been proposed a speeding up technique termed value reuse. This value reuse is arranged such that, an input value and an output value regarding a part of a program are registered in a reuse table, and when the same part is executed again, the registered output value is output if the input value is identical with the input value registered in the reuse table." (page 3, line 24 et seq.)

Moreover, pages 4-20 of Applicant's specification provide a further detailed background discussion of the concept and examples of performing reuse operations.

Regarding matching an input pattern with a pattern stored in the instruction region and conducting a value "resue" of output from previously executed instructions, see for example Applicant's specification at pages 73-83, discussing examples where an input pattern of address/values from a sequence of instructions is registered and matched in the form of a tree structure and pages 83-86 discussing examples for storing output values for reuse. For example, page 84, lines 2-8 explains that:

> "An input pattern is registered in the RF and RB, in the form of a tree structure. Whether or not reuse is feasible is determined in the line at the end of the tree structure, i.e. the line in which the ending flag E is registered. Therefore, the output operation for the reuse is realized by registering, in each line in which the ending flag E is registered, a

pointer to output value storage means that stores an output value to be outputted." (page 84, lines 2-8)

Regarding the 35 U. S. C. § 103(a) Rejection:

The rejection of claims1-17 under 35 U.S.C. §103(a) as allegedly being unpatentable over Miki (U.S. Patent No. 6,810,474) in view of Huang (U.S. Patent No. 4,943,909) is respectfully traversed.

The Miki reference is basically directed toward an arrangement for decreasing the overall usage and processing time of the ALU in an information processor (e.g., a microprocessor) which is set up to perform speculative execution of instructions where a dependency on reference data exists between instruction words. In a brief discussion of background prior art, Miki makes some references to the use a memory for storing the past execution results of an instruction which may be later output and used depending to some extent on whether or not consecutive or subsequent instructions have some degree of data dependency. However, the memory disclosed and discussed by Miki is not a "dependency relations information storage" as recited in Applicant's claims. In contrast to Miki's memory, Applicant's dependency relations information storage is a memory that is used to store "dependency relations" information regarding I/O data patterns for groups of instructions rather than for the storage only of past execution results. For at least this reason, Applicant respectfully contends that Miki does not teach and does not in the least bit suggest the use of such a "dependency relations storage" as set forth in Applicant's claims. Moreover, as the Office Action admits, Miki does not describe any details of how Applicant's claimed input and output elements are derived. (Office Action at page 11, para. 2.)

The Huang et al. reference is directed toward a processor having a specific hardware architecture that enables the performing of any computing function through the use of a regular

array of a plurality of interconnected processing elements (PEs). The Office Action presumably relies on Huang to supply details of Applicant's input/output group including input patterns and their associated output patterns and to teach the generating of dependency relations information as set forth in Applicant's claims. In doing so, the Office Action makes reference to Fig,. 3 and col. 5, lines 16-51 of the Huang reference. (Office Action at page 11.) However, as evident from Figure 3, this particular passage in Huang discloses only that a right input of each Processing Element (PE) in an array is physically connected to (i.e., "derived") from the left output of a PE from a preceding row in the same column, and that the left input of each PE is obtained from the right output of a PE of a preceding row in the left adjacent column. The disclosed explanations by Huang of physical interconnections of multiple Processing Elements has no relationship to the deriving or storing of dependency relationship information between input and output patterns of executed instructions groups in the manner as set forth in Applicant's independent claims. Consequently, for the sake of argument only, even if the teachings of Huang could be combined with the teachings of Miki, the result would certainly not be operable in the manner as set forth in Applicant's claims.

The Office Action fails to cite prior art that remedies the deficiencies of Miki as set forth above, or to suggest any motivation to modify Miki to arrive at the claimed invention. There is no objective teaching or disclosure anywhere in Huang of modifying the Miki system to provide a means for generating an I/O group which includes a dependency relations storage section or a means for generating dependency relations information that indicates which input element in an input pattern in an I/O group that each output element in an associated output pattern is derived, as set forth in Applicant's claims. Likewise, the Office Action has failed to provide any

objective basis that would have motivated one of skill in the art to modify Miki's system to provide Applicant's claimed data processing device.

For at least the above reasons, Applicant respectfully contends that Miki considered either alone or together with Huang et al., fails to teach or suggest Applicant's claimed use of a means for generating an I/O group which includes a dependency relations storage section or Applicant's claimed generating of dependency relations information that indicates which input element in an input pattern in an I/O group that each output element in an associated output pattern is derived.

Claims 2-17 are dependent on claim 1 and since neither Miki nor Huang suggest the features or operations as discussed above and set forth in Applicants' independent claim 1, it is respectfully submitted that dependent claims 2-17 are patentable over the combined teachings of these references.

Conclusion

As all objections and rejections raised in the Office Action have been addressed by the above Amendments and Remarks, it is respectfully submitted that the present application is in condition for allowance. Should there be any outstanding matters that need to be resolved, the Examiner is respectfully requested to contact Applicant's undersigned representative, using the telephone number listed below the signature line, to conduct an interview in an effort to expedite prosecution in connection with the present application.

The Commissioner is authorized to charge the undersigned's deposit account #14-1140 in whatever amount is necessary for entry of these papers and the continued pendency of the captioned application.

Respectfully submitted,

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